CAIMS

1. An interpolation circuit comprising:

oversampling operation unit for performing oversampling operation from zero-order hold input data; and

~~first~~ convolution operation unit for performing convolution operation on plural data obtained by said oversampling operation unit twice or more repeatedly,

characterized in that interpolated data is generated along a quadratic function curve passing through the integral multiples of the value of said input data.

2. An interpolation circuit, characterized by comprising:

oversampling operation unit for performing oversampling operation from zero-order hold input data;

~~second~~ convolution operation unit for performing convolution operation on plural first data obtained by said oversampling operation unit to calculate plural second data enveloped by a symmetrical trapezoid of the shape having an upside of substantially 0.5 times a width of original input data and a base of substantially 1.5 times the width; and

~~third~~ convolution operation unit for performing convolution operation on said plural second data obtained by said second convolution operation unit to calculate plural third data enveloped by a smooth quadratic function curve having the width of a base being substantially twice the width of original input data.

3. An interpolation circuit, characterized by comprising:

oversampling operation unit for performing oversampling operation from zero-order hold input data; and

~~fourth~~ convolution operation unit for performing convolution operation on plural data obtained by said oversampling operation unit to calculate plural data enveloped by an equilateral triangle having the width of a base being substantially twice the width of said input data.

4. An interpolation circuit, characterized by comprising:

oversampling operation unit for performing oversampling operation from zero-order hold input data with a sampling period of $2n \cdot T_1$ at a time interval of T_1;

~~fifth~~ first convolution operation unit for performing convolution operation of n phases by adding plural data obtained by said oversampling operation unit n times with the data shifted by the time interval of T_1 ; and

~~sixth~~ second convolution operation unit for performing convolution operation of n phases by adding plural data obtained by said fifth convolution operation unit n times with the data shifted by the time interval of T_1.

5. The interpolation circuit according to claim 4, characterized in that at least one of said ~~fifth~~ first and sixth second convolution operation unit comprises data holding unit for holding n pieces of data output from said oversampling operation unit while shifting, and addition unit for adding n pieces of data held in said data holding unit.

6. The interpolation circuit according to any one of claims 1 through 5, characterized by comprising data appending unit

for appending data having the symmetrical values proportional to the input data before and after said input data in the former stage of said oversampling operation unit.